What is claimed is:

1. A method for forming a metal oxide semiconductor field effect transistor (MOSFET), comprising:

providing a substrate comprising a layer of silicon germanium grown on an underlying silicon layer;

forming trenches in the silicon germanium layer to define an active region of the MOSFET;

forming isolations in the trenches, the isolations comprising a high thermal conductivity insulating material; and

forming a MOSFET on the substrate in the active region, the MOSFET comprising a layer of strained silicon formed on the silicon germanium in the active region.

2. The method claimed in claim 1, wherein the trench formed in the silicon germanium layer exposes the underlying silicon layer and the isolations contact the silicon layer.

3. The method claimed in claim 1, wherein the isolations comprise an oxide liner formed on sidewalls of the trench and wherein the high thermal conductivity insulating material of the isolations contacts the silicon layer.

4. The method claimed in claim 1, wherein the isolations comprise an oxide trench liner.

5. The method claimed in claim 1, wherein the high thermal conductivity insulating material has a thermal conductivity higher than the thermal conductivity of silicon.

6. The method claimed in claim 1, wherein the high thermal conductivity insulating material is silicon carbide.

7. The method claimed in claim 1, wherein forming the isolations comprises:

forming an oxide liner in the trenches;

forming a layer of silicon carbide over the substrate to fill the trenches; and

planarizing the silicon carbide to form the isolations in the trenches.

8. The method claimed in claim 1, wherein a strained silicon layer is formed on the silicon germanium layer prior to forming the trenches, and

wherein the trenches are formed in the strained silicon layer and the silicon germanium layer.

9. The method claimed in claim 1, wherein forming the MOSFET comprises:

forming a gate insulating layer on the strained silicon layer;

forming a gate conductive layer on the gate insulating layer; and

patterning the gate conductive layer to form a gate overlying a gate insulator.

10. The method claimed in claim 9, wherein forming the MOSFET further comprises:

forming a first spacer around the gate; and

implanting shallow source and drain extensions.

11. The method claimed in claim 10, wherein forming the MOSFET further comprises:

forming a second spacer around the first spacer; and

implanting deep source and drain regions,

wherein the second spacer serves as an implantation mask during implanting of the deep source and drain regions.

12. The method claimed in claim 11, wherein forming the MOSFET further comprises:

forming nickel silicide source and drain contacts and a nickel silicide gate contact.

13. The method claimed in claim 1, wherein the silicon germanium layer has a composition $Si_{1-x}Ge_x$, where x is in the range of 0.1 to 0.3.

14. A metal oxide semiconductor field effect transistor (MOSFET) device, comprising:

a substrate comprising a layer of silicon germanium grown on a layer of silicon and having a strained silicon channel region formed thereon;

a gate overlying the strained silicon channel region and separated from the strained silicon channel region by a gate insulator;

source and drain regions formed at opposing sides of the gate in the silicon germanium; and

shallow trench isolations formed in the silicon germanium layer and defining an active region of the MOSFET, the shallow trench isolations comprising a high thermal conductivity insulating material for dissipating heat generated in the active region of the MOSFET.

15. The device claimed in claim 14, wherein the shallow trench isolations extend through the silicon germanium layer to contact the silicon layer.

16. The device claimed in claim 14, wherein the shallow trench isolations conduct heat from the active region to the silicon layer.

17. The device claimed in claim 16, wherein the high thermal conductivity insulating material contacts the silicon layer.

18. The device claimed in claim 14, wherein the shallow trench isolations comprise an oxide trench liner and silicon carbide that fills the trench.

19. The device claimed in claim 14, wherein the high thermal conductivity insulating material has a thermal conductivity higher than the thermal conductivity of silicon.

20. The device claimed in claim 19, wherein the high thermal conductivity insulating material is silicon carbide.